

1 HIGH-SPEED COMMUNICATION SYSTEM
2 WITH A FEEDBACK SYNCHRONIZATION LOOP
3

4 Para Segaram

5 ABSTRACT OF THE DISCLOSURE

6 In a communications device having a physical layer device and a processing device
7 connected to the physical layer device, the number of input/output (I/O) ports required for
8 communication between the devices in the gigabit range is substantially reduced by
9 utilizing millivolt differential I/O drivers and receivers. In addition, a calibration
10 feedback loop synchronizes the data and clock signals on the processing device, thereby
11 eliminating the need to recover the clock on the processing device.

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